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Design and Implementation of Performance Improved Medical Signal Filters with and without Multiplier

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ABSTRACT

The digital filter can be done professionally with the compact area and reduced power with simplified multiplication arithmetic. More than Decades of years Computer aided analysis of ECG signal is getting with incredible quantity of work being carried out in the earth. This paper is a small work on our part in that track. ECG Electrocardiogram signal is most comely known familiar and used medical signal, the ECG signal is very responsive in nature, and still if small noise combined with actual signal the different properties of the signal changes, Data ruined with noise must either filtered or eliminated, filtering is important issue for design thought of real time health care process. This work presents a better FIR filter which can be designed in VLSI technique, with or without multiplier and has less power and area improvement.

Keywords: *FIR filter design; ARM processor; Multiplier; ECG;*

Introduction

In signal processing, the filter functions to remove the noise from the signal like random noise and also to extract the necessary parts of the signal like components within a precise range of frequency (Quan et al., 2009)[1]The design of the filters for specific application includes the coefficient calculation according to various criteria including sampling frequency, pass band and stop band frequency, filter order etc.

In future, the mobile phones and portable computing systems are anticipated to offer increased services, faster data rates and higher processing speeds at reduced power dissipation levels. This delivers us with an inspiration to explore new methods in low-complexity design of high-performance digital signal processing blocks which operate at lower power levels. Semiconductor technology today provides unprecedented level of device integration where several orders of millions of transistors can be packaged in a single chip using the state-of-the-art. The number is expected to grow steadily for many years.

Human bodies are continuously provides messages about fitness. This messages may be observed through body-structure-related devices that evaluate heart speed, blood stress, oxygen infiltration levels, blood glucose, nerve transmission, brain movement and so forth. Usually in the past, such observations are taken at clearly stated points in time and indicated in patient's chart. Doctors in fact observe a smaller amount than one percent of these values as they make their round and treatment are prepared based upon this chart readings

Bio-medical signal processing includes the study of these observations to offer helpful message upon which doctors can make conclusions. Engineers are finding new techniques to prepare these signals by means of a range of mathematical formulae and sets of computer commands. Functioning with conventional bio-measurement tools, the signals can be figured out by software-commands and provides the doctors , idea about what happening or viewable at present. By using more fancy (or smart) means to carefully study what bodies are saying, we can possibly decide the state of a patient's health through equipments which will not require cutting into the body.

Background

An extensive literature review was carried out on existing digital filters model and the method that are used for enhancing the performance of the digital filters.

Kucic et al.,(2001)[2]suggested a floating-gate technology based on adaptive filter which can be programmed. The author has carried out a basic review on floating-gate techniques and how this technique is programmed into adaptive filter circuits. The author has proposed a program filter method that can extend the capacity of the function and circuits. Furthermore, the author has demonstrated to expand our programmable channels as versatile channels both through weight bother strategies and constantly adjusting relationship rule techniques.

Yamada & Nishihara, (2001)adders and subtracters. The critical path is minimized by insertion of pipeline registers and is equal to the propagation delay of an adder. The number of pipeline registers is limited by using an equivalent transformation on a signal flow graph. The price paid for the 100% speedup is 5% increase in the area. The maximum sampling frequency is 78.6MHz.

Shahramian et al., (2012)[8] proposed Decision feedback equalizer (DFE) architectures with changing quantities of discrete-time taps and continuous time IIR filters are thought about for use in run of the mill wireline filters. For every situation, the DFE coefficients are enhanced to minimize a cost capacity that similarly weights both jitter and vertical eye opening. Notwithstanding when a few reflections are available persistent time IIR taps can be successful if their channel coefficients are appropriately enhanced. Utilizing a DFE engineering with just two IIR channels gives satisfactory outcomes to both a 26-dB misfortune persuade link and a 16 FR-4 back-plane channel at 10 Gb/s while keeping the DFE intricacy low. Moreover, the usage and exploratory aftereffects of a DFE with different (three) IIR channels is accounted for. Generated in a 0.13 μm CMOS handle, the DFE uses17.3 mW from a 1.2 V supply. A BER of 10−12 was accomplished at an information rate of 3.7 Gb/s.

Kamat et al.,(2010)[5] suggested dynamic resistor–capacitor (RC) channels utilizedoperation amps and its alteration by Moschytz are notable to dynamic RC filter designs. This utilization first-arrange all-pass organizes in a negative feedback loop. New present mode all inclusive operational trans conductance amplifier-capacitor (OTA-C) biquad channels in view of the TG dynamic RC channel was considered for this study. Furthermore, the author suggested that these depend on the proposed OTA-C based first-arrange all-passnetwork. Three diverse input plans were explored in the proposed digital filter structure to lessen the Q pole sensitivity. The proposed biquad channels are appeared to execute every single diverse sort of channels like low-pass, high-pass, band-pass, symmetric indent, all-pass, low-pass score and high-pass indent. The amalgamation of the general biquad is completed withnovelty by summoning the relationship with direct-frame advanced filter structures. The unique instance of all-pass digital filter acknowledgment got from the proposed global filter needs extra equipment for understanding the feed forward coefficients. Subsequently elective OTA-C based all-pass filter usage in view of Mitra–Hirano and Gray–Markel second-arrange computerized channel structures are inferred in which the coefficients that are utilized to understand the denominator are partaken in the acknowledgment of numerator. All the proposed circuits are contrasted and alternate structures accessible in the writing. The stimulation aftereffects of the proposed circuits was demonstrated.

Tsividis, (2010)[6]reviewed the event driven analog-to-digital conversion and related to digital signal processing techniques. The author suggests that techniquesare still in the research stage and can possibly lessen the utilization of energy and data transmission assets in a few critical applications.

Azim et al., (2011)[4] suggested most generally utilized digital channels are FIR channels that are typically implemented with the transversal structures. For FIR channel, the signal output is a direct mix of channel coefficients that generates a quadratic capacity (mean-square-error) along with the specific optimal operation point. FIR filter then again be acknowledged for getting changes in examination of transversal channel structure for speed of union, computational multifaceted nature and finite word length properties. IIR separating strategies display solid option for customary FIR sifting. The central favorable position of IIR channels is lesser parameterization to accomplish at standard execution of FIR channels. Moreover, the pole zero structures facilitate their displaying in physical frameworks.

C.Dai (2010)[10] proposed new parallel FIR filter structures, which are valuable to symmetric coefficients as far as the equipment cost, under the condition that the quantity of taps is a multiple of 2 or 3. The proposed parallel FIR structures exploits the innate way of symmetric coefficients lessening a large portion of the quantity of multipliers in sub channel segment to the detriment of extra adders in preprocessing and post handling squares. Trading multipliers with adders is favorable in light of the fact that adders weigh not as much as multipliers as far as silicon region; what's more,

the overhead from the extra adders in preprocessing and postprocessing squares remain settled and do not increment alongside the length of the FIR channel, though the quantity of lessened multipliers increments alongside the length of the FIR channel.

Implementation of FIR Filter

Multiplier based implementatio: A filter is employed to adjust the parameters of applied signal in order to meet our requirement.. A digital filter acts over digital data. (a series of 1&0s, obtained by the sampling and quantizing an analog data) also develops a digital data... These specifications, in linear convolution by the key in sequence provide the required yield. In the Figure.1, the multiplier part is represented with the Line and column bypassing multiplier.

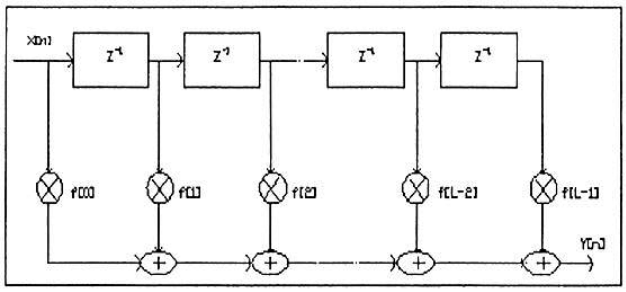

Figure 1: The FIR filter with order L

Comparison of FIR filters with Different multipliers: The Booth multiplier in which the multiplication of one of two pre determined value with a product takes place to get the result .Wallace tree multiplier is one which uses AND , half and full adders.FIR Filter can be constructed with bypassing multiplier instead of other multipliers the figure 2 shows the power consumption performance of different multipliers.

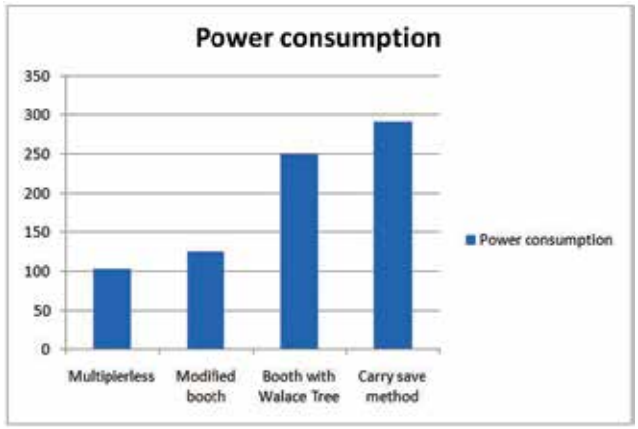

Figure 2: Power consumption Comparison of Multipliers

Multiplier Less Implementation:

ARM processor implementation of Proposed Medical signal filter: ARM Cortex M4 processor have an extremely superior set of multiply-combine commands that can execute more than one integer multiply-combine operation in one clock period (e.g. SMLAD), which leads them to perform better in digital signal processing.

The simple idea for building a digital filter is to employ Micro Modeler DSP, which gives a browser-based, self-sufficient filter design situation. Pull a filter to the function and visually organize the filter's frequency reaction. Once response is organized, copy and paste the robotically developed code into a .c and an h file and add to the project. All of the filters developed by Micro Modeler DSP utilize the equal interface, so it's simple to change to another filter with no change in present function code. It can be chosen to develop a code that uses C, CMSIS DSP libraries or mixed C and ARM Assembly depending on user preference.

This example explains the usage of the Code Replacement Library (CRL) for ARM processor with DSP blocks. The wave form is as shown in figure.3.

Task 1: Setup and Simulate

1. Open the ex_fir_ne10_tut_ml example function, which implements a lowpass FIR filter object.
2. Create two sine wave signals with 1KHz and 3KHz frequency, respectively.

```
sin1 = dsp.SineWave('Amplitude',1,'Frequency',1000,...
'SampleRate',8000, 'SamplesPerFrame', 76,...
'OutputDataType', 'single');
sin2 = dsp.SineWave('Amplitude',4,'Frequency',3000,...
```

'SampleRate',8000, 'SamplesPerFrame', 76,...

'OutputDataType', 'single');

3. Create a spectrum analyzer to view the spectrum of the input and filtered output.

scope = dsp.SpectrumAnalyzer('SampleRate',8e3,'ShowLegend',true,...

'PlotAsTwoSidedSpectrum', false, ...

'RBWSource', 'Property',...

'RBW',8000/260, 'Window','Kaiser', ...

'OverlapPercent', 80,...

'YLimits', [-76 56], 'SpectralAverages',10);

4. Simulate the example

NN = 2000;

for k = 1:NN

x1k = sin1(); % generate 1K Hz sine wave

x3k = sin2(); % generate 3K Hz sine wave

n1 = randn(size(x1k), 'single')*sqrt(.05); % generate noise signal

u1 = x1k+x3k+n1;

y1 = ex_fir_ne10_tut_ml(u1);

scope([u1,y1]);

end

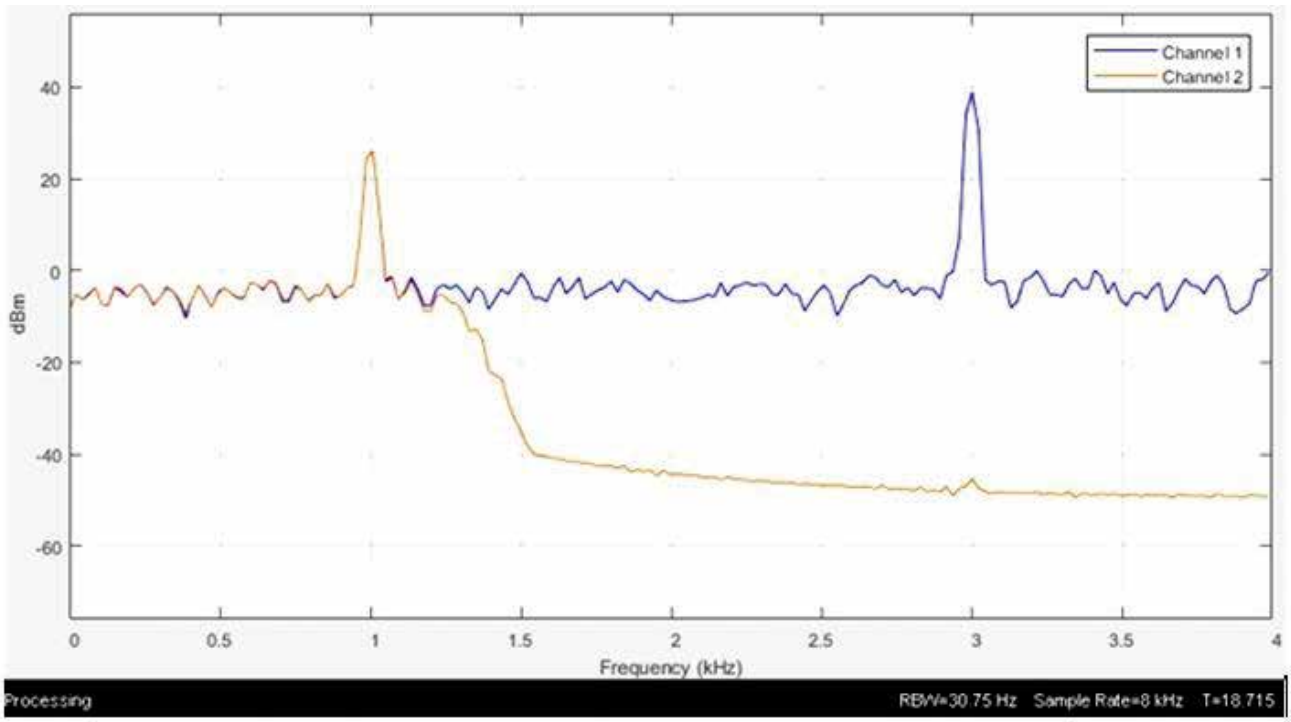

Figure 3. Output signal from Spectrum analyzer.

Task 2: Configure for Code Replacement

1. Create a code generation configuration object for use with codegen when generating a C/C++ static library.

   cfgEx = coder.config('lib');

   cfgEx.CodeReplacementLibrary = 'ARM Cortex-A';

   cfgEx.HardwareImplementation.ProdHWDeviceType = 'ARM Compatible->ARM Cortex';

   cfgEx.GenCodeOnly = true;

2. Open the **Custom Code** panel of the configuration dialog and verify the settings.

   cfgEx.dialog

Task 3: Generate code

1. Change your current folder in MATLAB to a temporary writable folder. Copy the MATLAB file to the temporary folder.

   tempdirObj = armcortexadstexample.dstTempdir('ex_fir_ne10_tut_ml_workflow');

   dstarmsrc = which('ex_fir_ne10_tut_ml');

   dstarmtmpdir = tempdirObj.tempDir;

   type(fullfile(dstarmsrc))

   copyfile(dstarmsrc, dstarmtmpdir, 'f');

   function y1 = ex_fir_ne10_tut_ml(u1)

   % Copyright 2014-2016 The MathWorks, Inc.

   %#codegen

   persistent fir;

   if isempty(fir)

   fir = dsp.FIRFilter('Numerator', fir1(63, 0.33));

   end

   y1 = fir(u1);

   end

2. Generate C code for the MATLAB function ex_fir_ne10_tut_ml.m.

   codegenex_fir_ne10_tut_ml-argssingle(u1)-configcfgEx-report

3. When code generation finishes successfully, click **View report** to display the code generation report.

4. Click on the ex_fir_ne10_tut_ml.c file. Notice the NE10 functions, **ne10_fir_init_float** and **ne10_fir_float_neon** in the ex_fir_ne10_tut_ml function.

Task 4: Verify the generated C code on target

The generated code can be compiled and executed on ARM Cortex-A target by using a user- selected tool chain.

Run the following code to delete the temporary directory.

status = tempdirObj.cleanUp;

Results and Discussion

Comparison with Multiplier based implementations: The improved multiplier less ARM processor implementation having less delay of only 10.2 ns and consumes only 102 mw power as Shown in Table 1and 2.

Tablel 1: Delay Comparison of similar methods

Methods	Delay ns.
Multiplier less method	10.2
Modified Booth	10.22
Modified Booth with Wallace Tree	8.9
Distributed Arithmetic	18.9
Distributed Arithmetic with Partition	16.804

Table 2: Power consumption Comparison of similar methods

Methods Table	Power consumption in mw.
Multiplier less Method	102
Modified Booth	125
Modified Booth with Wallace Tree	250
Carry save method	290

Medical signal Display and Transmission With ARM processor: If this proposed method is used in medical applications like filtering of ECG and other medical signals, due to the presence of ARM controller some other measurement, control ,display and transmission of the signal to some other remote location also can be done without additional processor.

The inputting and the handling of EMG signal is completed using LPC-2103 microcontroller unit. The LPC- 2103 is 32-bit ARM-7TDMIS processing unit, using on-time emulation that associates the microcontroller unit with 32 KB implanted quick flash memory. Owing to unit's miniature dimension and little power utilization, the LPC -2103 is perfect in areas wherever dimension is main constraint.

For monitoring heart activity the ECG signal is used. Our system is divided into three subsystems 1.ECG Acquisition 2.Processing in ARM7 3.GSM.This is real time system. In this project we will design for monitoring of ECG data using ARM7 LPC2148 and GSM module .Here first data is acquired using ARM7 which is further sent wirelessly using GSM. The device will be economical. It will be helpful for the patient and doctor for easy Monitoring. It will be less complex as compared to other technology. Less Power is required for its operation and control of the device. This device is used in Hospital, Military, Homecare Unit, and Sports Training.

The block diagram of this system is as shown in the figure 4.The hardware system consist of ECG acquisition, ARM7 processor and GSM module. In this system, ECG signal are acquired using 3 lead ECG electrodes .This signal are given to ARM7 processor for amplification and filtration.

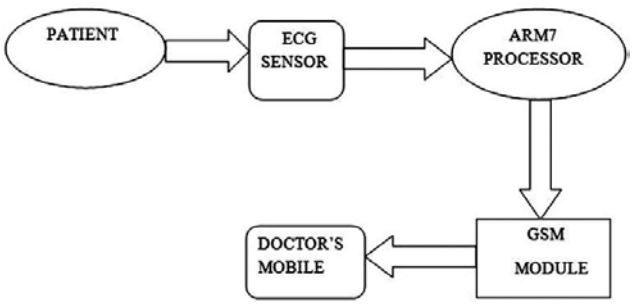

Figure 4: System block diagram

GSM (Global System for Mobile communication or Groupe Speciale Mobile) communications, initiated by the European Commission, is the second generation mobile cellular system aimed at developing .GSM is the world's most popular 2G technology. It was developed to solve the fragmentation problems of the first cellular system in Europe.GSM promised a wide range of network services through the use of ISDN. It also specifies digital modulation and network level architectures and services.

Conclusion

In this work we also projected and implemented a portable filter for real-time and personal purposes. We reduced the hardware complexity by using the digital filter-driven hardware architecture. According to the experimental results, the proposed filter with ARM processor has lower computational complexity than other existing filtering algorithms. The minimized number in hardware of this idea offers the benefit such as less consumption of space and power for overall system including signal transmission and display. As the ARM processor can also be used for signal transmission and display the revised filter has less delay and power.

Ethical Clearance: NA

Source of Funding: Self

Conflict of Interest: Nil

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